

**Remarks**

Claims 23-48 were rejected as unpatentable over KUDO et al. 6,853,037 in view of O 7,088,964 the admitted prior art (APA), and COMPTON et al. 6,462,929. Reconsideration and withdrawal of the rejection are respectfully requested.

Claim 23 provides, among other features, that the MOS varactor film (the second insulating film) is thinner than the thinnest of the MOS transistor films (the first insulating films), where the MOS transistor films have a plurality of different thicknesses. Thus, the second insulating film is thinner than all the first insulating films. The references do not disclose this. Claim 36 is similar.

KUDO et al. disclose a semiconductor device with a plurality of MOS transistors having different gate insulating film thicknesses. The film thickness of the n-channel high-voltage transistor is greater than the film thickness of the p-channel high voltage transistor, which is greater than the film thickness of the low-voltage transistor (Abstract). KUDO et al. do not disclose a film thickness of a varactor.

O discloses that CMOS varactors are generally formed using design rules for logic devices and that logic devices are generally significantly smaller than I/O devices and use a thinner gate oxide (column 11, lines 17-21). That is, the film thickness of the I/O transistor is thicker than that of the film

thickness of a logic transistor, and the film thickness of the varactor is equal to that of the logic transistor.

The APA acknowledges that logic devices and I/O devices are generally formed on the same chip.

Thus, KUDO et al. disclose only the film thicknesses of the transistors, and O discloses that the logic transistor has a film thickness equal to that of the varactor. Combining the references does not suggest to the artisan that the film thicknesses of all the MOS transistors are each to be greater than that of the varactor.

That is, the combination of these three references disclose that in a chip with logic devices and I/O devices, the thinnest gate insulating films among the MOS transistors is to be found in the logic devices. The combination merely discloses that the gate insulating film of the varactors element is the same thickness as that of a gate insulating film of the thinnest MOS transistor on the chip. There is nothing in the combination that discloses that the thickness of the second gate insulating film in the varactor element is thinner than the thinnest gate insulating film among the first gate insulating films of the MOS transistors with different thicknesses.

The above arguments were presented in a Pre-Appeal Brief and the application was returned to reopen prosecution. COMPTON et al. is newly-cited.

Figure 11 of COMPTON et al. is reproduced below; this figure shows a capacitor structure.

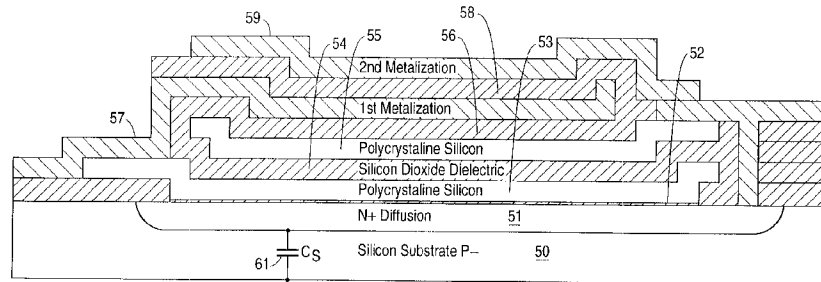


FIG. 11

This structure includes:

- a p-substrate 50,
- an N+ buried layer 51,
- a tunnel oxide silicon oxide layer 52 less than about 100 Angstroms thick and preferably 80 Angstroms thick,
- a first polysilicon layer 53 about 300 Angstroms thick,
- a second silicon dioxide layer 54 about 300 Angstroms thick,
- a second polysilicon layer 55,
- a third silicon dioxide layer 56 several hundred Angstroms thick,
- a first metallization layer 57,
- a fourth silicon dioxide layer 58 several hundred Angstroms thick, and
- a second metallization layer 59.

The capacitor with this structure provides:

that the capacitance of the tunnel oxide silicon oxide layer 52 is approximately  $3 \text{ fF}/\mu\text{m}^2$ ,

that the total capacitance is approximately  $4 \text{ fF}/\mu\text{m}^2$ , and

that the capacitance of the MOS transistor is  $0.08 \text{ fF}/\mu\text{m}^2$ .

From this, one assumes that the Official Action contends that COMPTON et al. disclose a MOS varactor, whose capacitance is that of the tunnel oxide silicon oxide layer 52, and that has an insulating film thinner than a gate insulating film of the MOS transistor (presumed from the capacitance per unit area.)

However, the capacitor disclosed in Figure 11 is a capacitor with a constant capacitance; it is not a varactor. A depletion layer is formed in the N+ buried layer 51 due to a high impurity concentration therein, which means that the capacitance is essentially constant. In the capacitor structure of Figure 11, the applied voltage is limited to about 1 volt in order to reduce the leak current of the tunnel oxide layer. In this voltage range, the capacitance is essentially constant. One of skill in the art would recognize this and see that COMPTON et al. do not disclose a MOS varactor that has an insulation film thinner (as presumed from the capacitance per unit area) than a gate insulating film of a MOS transistor.

Accordingly, the claims avoid the rejections under §103.

The claims avoid the rejections for yet a further reason. COMPTON et al. disclose that the tunnel oxide silicon oxide layer 52 has a film thickness of 80 Angstroms and a capacitance per

unit area of  $3 \text{ fF}/\mu\text{m}^2$ , and a MOS transistor with a capacitance per unit area of  $0.08 \text{ fF}/\mu\text{m}^2$ .

Based on the assumption that the capacitance per unit area is inversely proportional to the film thickness, the film thickness of the MOS transistor is 3000 Angstroms. An insulating film with this thickness is not normally used in a MOS transistor. One of skill in the art would see this, and recognize that the film thickness cannot be presumed simply from the comparison of the capacitance per unit area.

Further, the capacitance of a MOS transistor has C-V characteristics, meaning that the capacitance of a MOS transistor changed with respect to the voltage  $V_g$  applied to a gate electrode. This also demonstrates that the film thickness cannot be presumed simply from a comparison of capacitance per unit area.

Thus, the claims avoid the rejections under §103 for these further reasons.

New claims 49-50 have been added. Consideration and allowance of these claims are respectfully requested. The new claims provide that the MOS type varactor element has only one insulating film. By contrast, COMPTON et al. disclose that the capacitor has a laminated structure whose purpose is to increase the capacitance per unit area. There is no suggestion to use the single insulating film in the new claims.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

Please charge the claim fee of \$104 for two extra dependent claims added herewith to our credit card.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON

/Thomas W. Perkins/

Thomas W. Perkins, Reg. No. 33,027  
209 Madison Street, Suite 500  
Alexandria, VA 22314  
Telephone (703) 521-2297  
Telefax (703) 685-0573  
(703) 979-4709

TWP/lrs